



**PI74FCT16543T  
PI74FCT162543T  
PI74FCT162H543T**

**Fast CMOS 16-Bit  
Latched Transceivers**

**Product Features:**

**Common Features:**

- PI74FCT16543T, PI74FCT162543T and PI74FCT162H543T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 300 mil wide plastic SSOP (V)

**PI74FCT16543T Features:**

- High output drive:  $I_{OH} = -32\text{ mA}$ ;  $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit “live insertion”
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1.0V$  at  $V_{CC} = 5V, T_A = 25^\circ C$

**PI74FCT162543T Features:**

- Balanced output drivers:  $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.6V$  at  $V_{CC} = 5V, T_A = 25^\circ C$

**PI74FCT162H543T Features:**

- Bus Hold retains last active state during 3-state
- Eliminates the need for external pull-up resistors

**Product Description:**

Pericom Semiconductor’s PI74FCT series of logic circuits are produced in the Company’s advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

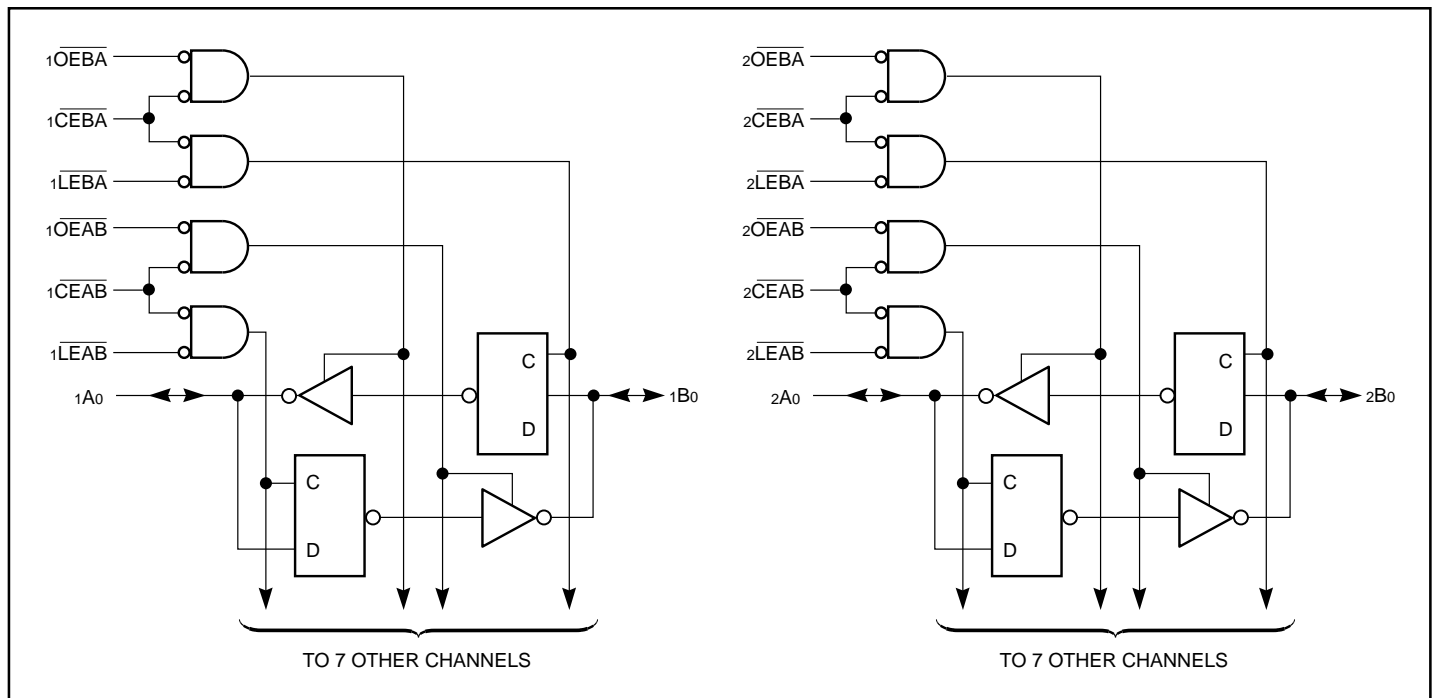
The PI74FCT16543T, PI74FCT162543T and PI74FCT162H543T are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{xCEAB}$ ) input must be LOW in order to enter data from  $xAx$  or to take data from  $xBx$ , as indicated in the Truth Table. With  $\overline{xCEAB}$  LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{xLEAB}$  signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With  $\overline{xCEAB}$  and  $\overline{xOEAB}$  both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{xCEBA}$ ,  $\overline{xLEBA}$ , and  $\overline{xOEBA}$  inputs.

The PI74FCT16543T output buffers are designed with a Power-Off disable allowing “live insertion” of boards when used as backplane drivers.

The PI74FCT162543T has  $\pm 24\text{ mA}$  balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H543T has “Bus Hold” which retains the input’s last state whenever the input goes to high-impedance preventing “floating” inputs and eliminating the need for pull-up/down resistors.

**Logic Block Diagram**



### Product Pin Description

Pin Name	Description
$\overline{xOEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{xOEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{xCEAB}$	A-to-B Enable Input (Active LOW)
$\overline{xCEBA}$	B-to-A Enable Input (Active LOW)
$\overline{xLEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{xLEBA}$	B-to-A Latch Enable Input (Active LOW)
$xAx$	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
$xBx$	B-to-A Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
GND	Ground
Vcc	Power

**Note:** 1. For the PI74FCT162H543T, these pins have “Bus Hold.” All other pins are standard, outputs, or I/Os.

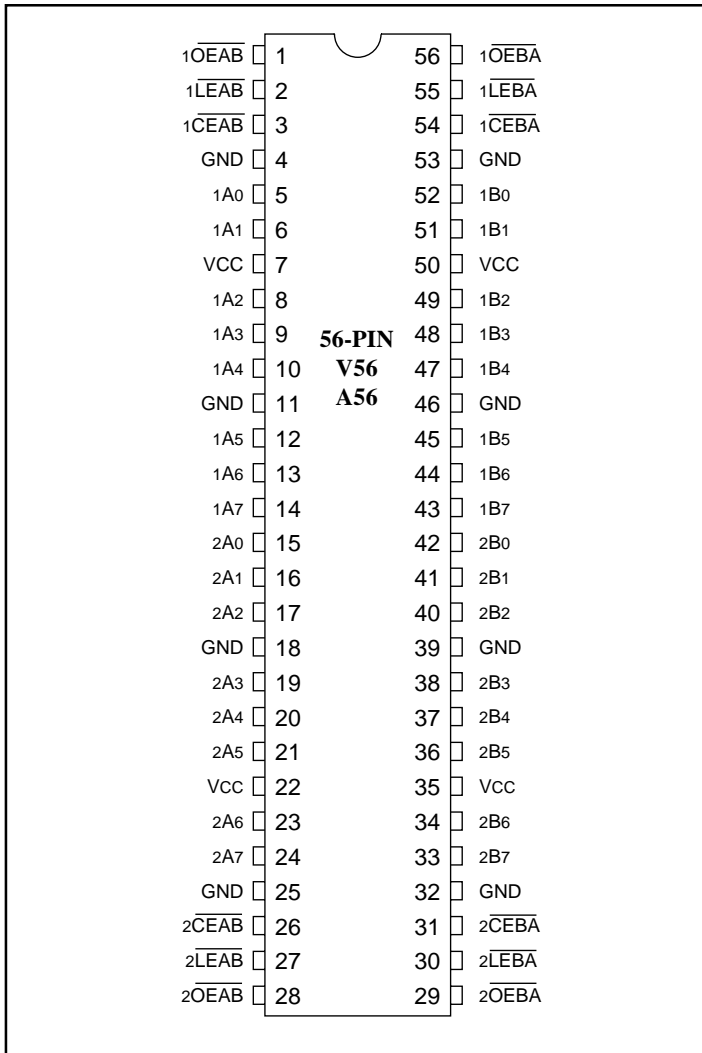
### Truth Table<sup>(1)</sup>

Inputs			Latch Status	Output Buffers
$\overline{xCEAB}$	$\overline{xLEAB}$	$\overline{xOEAB}$	$xAx$ TO $xBx$	$xBx$
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

#### Notes:

- \*Before  $\overline{xLEAB}$  LOW-to-HIGH Transistion  
H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care or Irrelevant  
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using  $\overline{xCEBA}$ ,  $\overline{xLEBA}$ , and  $\overline{xOEBA}$ .

### Product Pin Configuration



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V <sub>CC</sub> Only) .....	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current .....	120mA
Power Dissipation .....	1.0W

#### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC Electrical Characteristics (Over the Operating Range, T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 10%)

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I <sub>IH</sub>	Input HIGH Current	Standard Input, V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub>			1	μA
I <sub>IH</sub>	Input HIGH Current	Standard I/O, V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub>			1	μA
I <sub>IH</sub>	Input HIGH Current	Bus Hold Input <sup>(4)</sup> , V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub>			±100	μA
I <sub>IH</sub>	Input HIGH Current	Bus Hold I/O <sup>(4)</sup> , V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub>			±100	μA
I <sub>IL</sub>	Input LOW Current	Standard Input, V <sub>CC</sub> = Min.	V <sub>IN</sub> = GND			-1	μA
I <sub>IL</sub>	Input LOW Current	Standard I/O, V <sub>CC</sub> = Min.	V <sub>IN</sub> = GND			-1	μA
I <sub>IL</sub>	Input LOW Current	Bus Hold Input <sup>(4)</sup> , V <sub>CC</sub> = Min.	V <sub>IN</sub> = GND			±100	μA
I <sub>IL</sub>	Input LOW Current	Bus Hold I/O <sup>(4)</sup> , V <sub>CC</sub> = Min.	V <sub>IN</sub> = GND			±100	μA
I <sub>BHH</sub>	Bus Hold	Bus Hold Input <sup>(4)</sup> , V <sub>CC</sub> = Min.	V <sub>IN</sub> = 2.0V	-50			μA
I <sub>BHL</sub>	Sustain Current		V <sub>IN</sub> = 0.8V	+50			
I <sub>OZH</sub> <sup>(5)</sup>	High-Impedance	V <sub>CC</sub> = Max.	V <sub>OUT</sub> = 2.7V			1	μA
I <sub>OZL</sub> <sup>(5)</sup>	Output Current (3-STATE OUTPUTS)	V <sub>CC</sub> = Max.	V <sub>OUT</sub> = 0.5V			-1	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA			-0.7	-1.2	V
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>OUT</sub> = GND		-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>OUT</sub> = 2.5V		-50		-180	mA
V <sub>H</sub>	Input Hysteresis				100		mV

#### Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

**PI74FCT16543T Output Drive Characteristics** (Over the Operating Range)

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3.0 mA	2.5	3.5		V
			I <sub>OH</sub> = -15.0 mA	2.4	3.5		
			I <sub>OH</sub> = -32.0 mA	2.0	3.0		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 64 mA		0.2	0.55	V
I <sub>OFF</sub>	Power Down Disable	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>OUT</sub> ≤ 1.5V		—	—	±100	μA

**PI74FCT162543T/162H543T Output Drive Characteristics** (Over the Operating Range)

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -24.0 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 24 mA		0.3	0.55	V
I <sub>ODL</sub>	Output LOW Current	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V <sup>(3)</sup>		60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V <sup>(3)</sup>		-60	-115	-150	mA

**Capacitance** (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameters <sup>(4)</sup>	Description	Test Conditions	Typ	Max.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF

**Notes:**

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND or V <sub>CC</sub>		0.1	500	μA
ΔI <sub>CC</sub>	Supply Current per Input @ TTL HIGH	V <sub>CC</sub> = Max.	V <sub>IN</sub> = 3.4V <sup>(3)</sup>		0.5	1.5	mA
I <sub>CCD</sub>	Supply Current per Input per MHz <sup>(4)</sup>	V <sub>CC</sub> = Max., Outputs Open x $\overline{\text{CEAB}}$ & x $\overline{\text{OEAB}}$ = GND x $\overline{\text{CEBA}}$ = V <sub>CC</sub> One Bit Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		60	100	μA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 10 MHz 50% Duty Cycle x $\overline{\text{LEAB}}$ , x $\overline{\text{CEAB}}$ , and x $\overline{\text{OEAB}}$ = GND x $\overline{\text{CEBA}}$ = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		0.6	1.5 <sup>(5)</sup>	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND		0.9	2.3 <sup>(5)</sup>	
		V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 2.5 MHz 50% Duty Cycle x $\overline{\text{LEAB}}$ , x $\overline{\text{CEAB}}$ , and x $\overline{\text{OEAB}}$ = GND x $\overline{\text{CEBA}}$ = V <sub>CC</sub> 16 Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		2.4	4.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND		6.4	16.5 <sup>(5)</sup>	

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$
I<sub>CC</sub> = Quiescent Current  
ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
D<sub>H</sub> = Duty Cycle for TTL Inputs High  
N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
f<sub>i</sub> = Input Frequency  
N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
All currents are in milliamps and all frequencies are in megahertz.

### PI74FCT16543T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	16543T		16543AT		16543CT		16543DT		16543ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tpZH tpZL	Output Enable Time xOEBA or xOEAB to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> xOEBA or xOEAB to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	2.0	—	2.0	—	2.0	—	1.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tw	xLEAB or xLEBA Pulse Width 5.0 LOW <sup>(3)</sup>		—	5.0	—	5.0	—	3.0	—	3.0	—	3.0	ns
tsk(o)	Output Skew <sup>(4)</sup>		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

### PI74FCT162543T Switching Characteristics over Operating Range

Parameters	Description	Conditions <sup>(1)</sup>	162543T		162543AT		162543CT		162543DT		162543ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tpZH tpZL	Output Enable Time xOEBA or xOEAB to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> xOEBA or xOEAB to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	2.0	—	2.0	—	2.0	—	1.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tw	xLEAB or xLEBA Pulse Width 5.0 LOW <sup>(3)</sup>		—	5.0	—	5.0	—	3.0	—	3.0	—	3.0	ns
tsk(o)	Output Skew <sup>(4)</sup>		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

**Notes:**

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction.  
This parameter is guaranteed by design.

**PI74FCT162H543T Switching Characteristics over Operating Range**

Parameters	Description	Conditions <sup>(1)</sup>	162H543T		162H543AT		162H543CT		162H543DT		162H543ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tpZH tpZL	Output Enable Time xOEBA or xOEAB to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time <sup>(3)</sup> xOEBA or xOEAB to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	2.0	—	2.0	—	2.0	—	1.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tw	xLEAB or xLEBA Pulse Width 5.0 LOW <sup>(3)</sup>		—	5.0	—	5.0	—	3.0	—	3.0	—	3.0	ns
tsk(o)	Output Skew <sup>(4)</sup>		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

**Notes:**

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.